Notice of Allowability	Application No.	Applicant(s)	
	09/987,317	AKITA, YOHEI	
	Examiner	Art Unit	
	Fred Ferris	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *12 September 2005*.

2. ☒ The allowed claim(s) is/are *1-20*.

3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

1. Claims 1-20 have been presented for examination based on applicant's amendment filed on 12 September 2005. Amended claims 1-20 have now been allowed over the prior art of record.

Response to Arguments

2. Applicant's arguments filed 12 September 2005 have been fully considered and are persuasive.

Regarding applicants response to 112(1) rejection: The examiner withdraws the 112(1) rejection in view of applicant's amendment to the claims.

Regarding applicant's response to 102(b) and 103(a) rejection: The examiner withdraws the 102(b) and 103(a) rejections in view of applicants amendment to the claims and arguments submitted 12 September 2005. In particular, applicants have amended the claims to require an output vector being applied from an outside entity through a communication line at the beginning of subsequent time steps, and clarified the process of monitoring internals states as input vectors are applied during subsequent time steps. (As noted in examiners previous rejection, simply dividing the simulation into discrete time steps and monitoring internals states as input vectors are applied would be inherently performed by nearly any logic simulation. Such systems would also obviously include a communication line, i.e. Network/Internet) However, applicants have now clarified that the verification model recited in the amended claims, requires transmitting an (in-house) input vector for each module of the outside entity to

the outside entity at one time step through the communication line (e.g., an exchange communication line, the Internet, or exclusive line, as in the Fig. 1), such that the outside entity simulates operation of each module with the input vector at the one time step so as to compute an output vector, and further receives the output vector from the outside entity through the communication line at a beginning of the subsequent time step, and subsequently integrates the output vectors from all modules at the subsequent time step to obtain an output of the whole system at the subsequent time step. (See: Figures 3-7, for example) Hence, the examiner concurs that the specific sequences of steps relating to the time step based process of simulating module operation with input/output vectors communicated between the in-house and outside entity (i.e. synchronization between in-house and outside entities) as now required by amended claims 1, 2, and 7, is not explicitly disclosed or rendered obvious by the prior art.

Allowable Subject Matter

3. *Claims 1-20 are allowed over the prior art of record.*

The following is an examiner's statement of reasons for allowance:

Applicants are disclosing a method and system for a system verification method for verifying the operation of system design modules that are protected as intellectual property including providing design data for a verification module, simulating system operation to obtain an output, supplying input vectors to modules, computing output vectors based on a verification module, and integrating output vectors. This has been

disclosed in the prior art of record.

While these elements are individually disclosed in the prior art, the prior art of record does not meet the conditions as suggested in MPEP section 2132, namely:

"The identical invention must be shown in as complete detail as is contained in the ... claim." Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). The elements must be arranged as required by the claim, but this is not an ***ipsissimis verbis*** *test, i.e., identity of terminology is not required.* ***In re Bond,*** *910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990)."*

In particular, the prior art does not disclose the specific sequence of steps relating to the verification model requiring transmitting of an (in-house) input vector for each module of an outside entity to the outside entity at one time step through a communication line (e.g., an exchange communication line, the Internet, or exclusive line, as in the Fig. 1), such that the outside entity simulates operation of each module with the input vector at the one time step so as to compute an output vector, and further receive the output vector from the outside entity through the communication line at a beginning of the subsequent time step, and subsequently integrating the output vectors from all modules at the subsequent time step to obtain an output of the whole system at the subsequent time step (See: Figures 3-7, for example) as now recited in independent claims 1 and 2. The closest prior art uncovered during examination teaches certain limitations of the claimed invention as follows:

U.S. Patent 6,446,243 issued to Huang et al: teaches a system verification method for verifying the operation of system design modules that are protected as

intellectual property including providing design data for a verification module, simulating system operation to obtain an output, supplying input vectors to modules, computing output vectors based on a verification module, and integrating output vectors. However, Huang does not explicitly disclose the specific sequence of steps relating to the verification model requiring transmitting of an (in-house) input vector for each module of an outside entity to the outside entity at one time step through a communication line, such that the outside entity simulates operation of each module with the input vector at the one time step so as to compute an output vector, and further receive the output vector from the outside entity through the communication line at a beginning of the subsequent time step, and subsequently integrating the output vectors from all modules at the subsequent time step to obtain an output of the whole system at the subsequent time step (See: Figures 3-7, for example) as now recited in independent claims 1 and 2.

U.S. Patent 6,782,511 issued to Frank et al: teaches a behavioral model simulation tool hosted privately on a webserver that tests and validates a system design while executing in a secure business-to-business environment of an application service provider where the validated solution is downloaded over the Internet. However, Frank again does not explicitly disclose the specific sequence of steps relating to the verification model requiring transmitting of an (in-house) input vector for each module of an outside entity to the outside entity at one time step through a communication line, such that the outside entity simulates operation of each module with the input vector at the one time step so as to compute an output vector, and further receive the output vector from the outside entity through the communication line at a beginning of the

subsequent time step, and subsequently integrating the output vectors from all modules at the subsequent time step to obtain an output of the whole system at the subsequent time step (See: Figures 3-7, for example) as now recited in independent claims 1 and 2.

Independent claims 2 and 7 further use "means for" language and are given deference in view of In re Donaldson and interpreted in view of 35 U.S.C. § 112 paragraph 6. The "means for" language and the limitations related thereto of claims 2 and 7 are interpreted within the scope of enablement as provided within the relative embodiment provided within applicant's specification. In particular, the specific "means for" limitations as recited in the claims is interpreted as defined by the specification as follows:

- means for simulating: (page 15, line , to 16, line 5, page 23, lines 20, , Fig. 2)

- means for dividing simulation time: (page 16, line 4 to 22, line 12, Figs. 3-8)

- means for supplying input vector: (pages 16-27, Figs. 4-8)

- means for computing (sending) output vector: (pages 16-27, Figs. 4-8)

- means for transmitting input vector: (pages 16-27, Figs. 4-8)

- means for receiving output vector: (pages 16-27, Figs. 4-8)

- means for integrating: (page 11, line 1 to 12, 15)

- means for repeating (controlling above): (pages 14-29, Figs. 2-8)

The features noted above therefore render the claimed invention non-obvious over the prior art of record. Dependent claims 3-6 and 8-20 are deemed allowable as depending from independent claims 2 and 7 respectively.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fred Ferris whose telephone number is 571-272-3778 and whose normal working hours are 8:30am to 5:00pm Monday to Friday. Any inquiry of a general nature relating to the status of this application should be directed to the group receptionist whose telephone number is 571-272-3700. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamini Shah can be reached at 571-272-2279. The Official Fax Number is: (703) 872-9306

Fred Ferris, Patent Examiner
Simulation and Emulation, Art Unit 2128
U.S. Patent and Trademark Office
Randolph Building, Room 5D19
401 Dulany Street
Alexandria, VA 22313
Phone: (571-272-3778)
Fred.Ferris@uspto.gov
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